·2/4 channel synchronous sampling，2/4 channel synchronous playback

·200/250Msps per channel，16bit

·Input bandwidth DC-100/120MHz

·Input range: can be set as ±1V、±2V、±5V、±10V

·Input impedance: 50Ω/1MΩ

·Output range: ±10V

·Multiple Communication Interfaces Available

·support FPGA secondary development

·Software development package supports C/C++，LabVIEW，Matlab etc

Series	Category	Resolution	Channel	Sampling Rate	Bandwidth	Storage depth	System support
LD735x-xx16	AD	16bit	2/4 channel	200/250Msps	DC-100/120MHz	2GB	Windows Linux
	DA	16bit	2/4 channel	250Msps	DC-50MHz		

Brief introduction

·LD735x-xx16 is Mysoow's "Agile" series acquisition and playback device, supporting 2/4 channel, 16bit， achieving 200/250Msps synchronous sampling，On board DDR3 memory granules, with 2GB storage volume，larger volume customization is also supported.

·Multiple interface buses are available, with optional support for RJ45, USB 3.0, and 10G optical ports.

·Support multiple triggering modes including hardware，triggering, software triggering and manual triggering etc. Continuous sampling mode is also supported.

·Support the secondary development for users, providing DLL dynamic link pool.

·Equipped with host computer Demo software, supporting the configuration of board and real-time display and storage of data.

Typical applications

·Optical Coherence Tomography（OCT）

·Non-destructive detection

·Ware form recorder

·Multi-channel transient recorder

Detailed parameters

Terminal	
Simulated input	2/4 channel，standard SMB interface，SSMA optional
Simulated output	2/4 channel，standard SMB interface，SSMA optional
Triggered input	1 way SMB
Triggered output	1 way SMB
Synchronous clock input	1 way SMB
Synchronous clock output	1 way SMB
IO Resources 2.0 12P box	4 sets of IO, 3.3V/5V level software switchable, capable of external power supply. Optionally configurable with 2 sets of MLVDS or 2 sets of RS485 (can constitute RS422 interface).
Communication bus	Optional Gigabit Ethernet port, USB 3.0 interface, and 10G optical port.
Acquisition system	
Resolution	16bit
Bandwidth	DC-100/120MHz
Input channel	2/4/6 channel synchronous sampling
Sampling rate	up to 200/250Msps
Sampling mode	Continuous sampling, finite point sampling
Full range input scope	±1V、±2V、±5V、±10V
Input coupling	DC/AC Switching
Input impedance	50Ω/1MΩ
Extreme input	±40Vmax
Playback system	
Resolution	16bit
Bandwidth	DC-50MHz
Output channel	2/4 channel synchronous playback
Sampling rate	250Msps
Maximum input data speed	250Msps
Playback mode	Real-time mode, buffering mode
Wave form	DDC mode(single sound mode)，AWG mode(any wave form mode)
Wave form output mode	DDS mode(single sound mode)，AWG mode(any wave form mode)
Full range output scope	±10V
Coupling means	DC coupling
Output impedance	50Ω

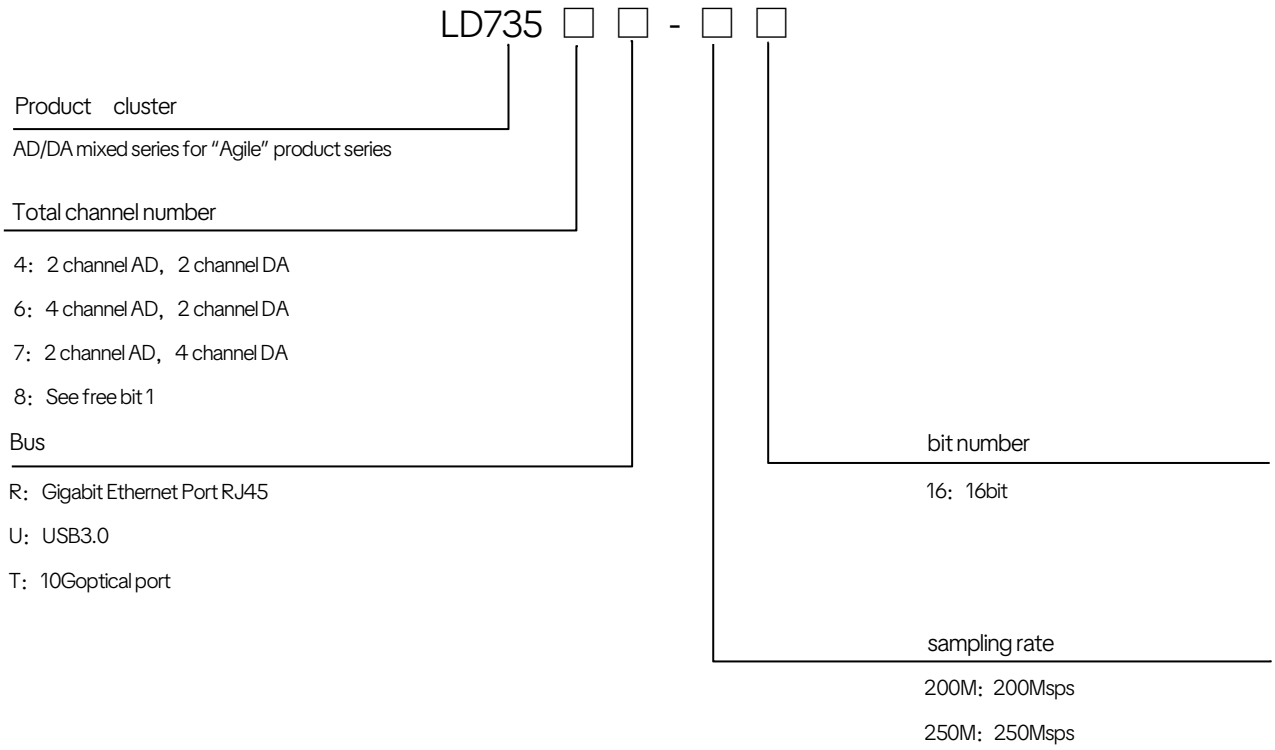
Storage						
Storage volume	2GB					
Recording capability	Can be set up by software，the overall volume does not exceed memory space					
Trigger depth	Can be set up by software, the overall volume does not exceed memory space					
Index parameter						
Input impedance	Gear	SNR	SINAD	SFDR	ENOB	Test conditions
50Ω	±2V	72	72	75	11.4	Input signal amplitude-1dBFS，frequency 1MHz，sampling rate 200M/250Msps
1MΩ	±2V	70	70	72	10.8	
Trigger Input System						
Trigger source	Software trigger, threshold(channel) trigger, external(simulation and digital) trigger					
Channel number	1 channel, supporting simulation and digital TTL, LVTTL，Input impedance 1MΩ					
Trigger input level	Simulation input ±0.2V~±5V, standard digital TTL, LVTTL level，square wave/pulse wave/trapezoidal wave					
Trigger frequency	≤2MHz					
Trigger mode	post-trigger, pre-trigger, delay-trigger, rising edge trigger, falling edge trigger, double-sided edge trigger					
Trigger threshold adjustment	±0.2V~±5V precisely adjustable					
Trigger input width	≥50ns					
Trigger delay	0~2^31 sampling cycle					
Trigger output						
Trigger output channel	1 channel，share terminal with clock output					
Trigger output level	LVTTL，output current 10mA					
Trigger output width	≥50ns，adjustable pulse width					
Clock system						
Clock source	Internal/external/external direct sampling clock source					
Feature of internal clock	10MHz，±2ppm					
External input clock amplitude	0.4Vpp ~ 3.3Vpp sine wave or square wave					

External input impedance	50Ω
External input coupling mode	AC coupling
External input frequency range	10MHz，1MHz~maximum sampling rate@external direct sampling mode
Clock output	10MHz@LVTTL，same source as sampling clock
Power requirements	
Power supply mode	Adapter-powered or Powered by adapter，DC005 2.0mm
Power requirement	Rated Voltage 12V, Supports 12~24V Input
Size and weight	
Size	length×width×height：200×127×48mm
Weight	~0.76kg
Environment parameters	
Working temperature	0℃ ~ +50℃
Relative working humidity	10% ~ 90%RH, no condensation
Storage temperature	-40℃ ~ +85℃
Relative storage humidity	5% ~ 95%RH, no condensation

Software Development Package

Provide software development package to help users to quickly accomplish application development and integration. MSDK software development package is applicable for Windows, Linux and other operation system, supporting the secondary integration and development for C/C++, Matlab, Labview, Python, C#, QT and other software, including host computer software, interface pool, DEMO routine and development description documents etc.

Order naming rules



Note:

1. The product is not equipped with coaxial cables by default, and our company can provide customized wire services

Chengdu Mysoow Electric Co.,LTD
Tel: +86-028-87409729
Whats: 8617348137889
Wechat: 17348137889
E-Mail:marketing@mysoow.com
Address: 1st Floor, Building B, No. 3 Tianhong Road,
High-tech West District, Chengdu, Sichuan Province, China
Website: www.mysoow-global.com